**ECEN 714-612 Lab 3**

1. cell18.spi

| //Spice netlist for an invertersimulator lang=spectresubckt IV (input output VDD VSS) parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u M1 output input VDD VDD tsmc18P w=wp l=lp M2 output input VSS VSS tsmc18N w=wn l=lnends IVsubckt NAND2 (A B output VDD VSS) parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u M1 output A VDD VDD tsmc18p w=wp l=lp M2 output B VDD VDD tsmc18p w=wp l=lp M3 output A n1 VSS tsmc18n w=wn l=ln M4 n 1 B VSS VSS tsmc18n w=wn l=lnendssubckt XOR2 (A B output VDD VSS) parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u Ainv (A Abar VDD VSS) IV wp=wp lp=lp wn=wn ln=ln Binv (B Bbar VDD VSS) IV wp=wp lp=lp wn=wn ln=ln M1 n13 B VDD VDD tsmc18p w=wp l=lp // B pmos M2 n24 Bbar VDD VDD tsmc18p w=wp l=lp // Bbar pmos M3 output Abar n13 VDD tsmc18p w=wp l=lp // Abar pmos M4 output A n24 VDD tsmc18p w=wp l=lp // A pmos M5 output Abar n57 VSS tsmc18n w=wn l=ln // Abar nmos M6 output A n68 VSS tsmc18n w=wn l=ln // A nmos M7 n57 Bbar VSS VSS tsmc18n w=wn l=ln // Bbar nmos M8 n68 B VSS VSS tsmc18n w=wn l=ln // B nmosends |
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1. simcap.spi

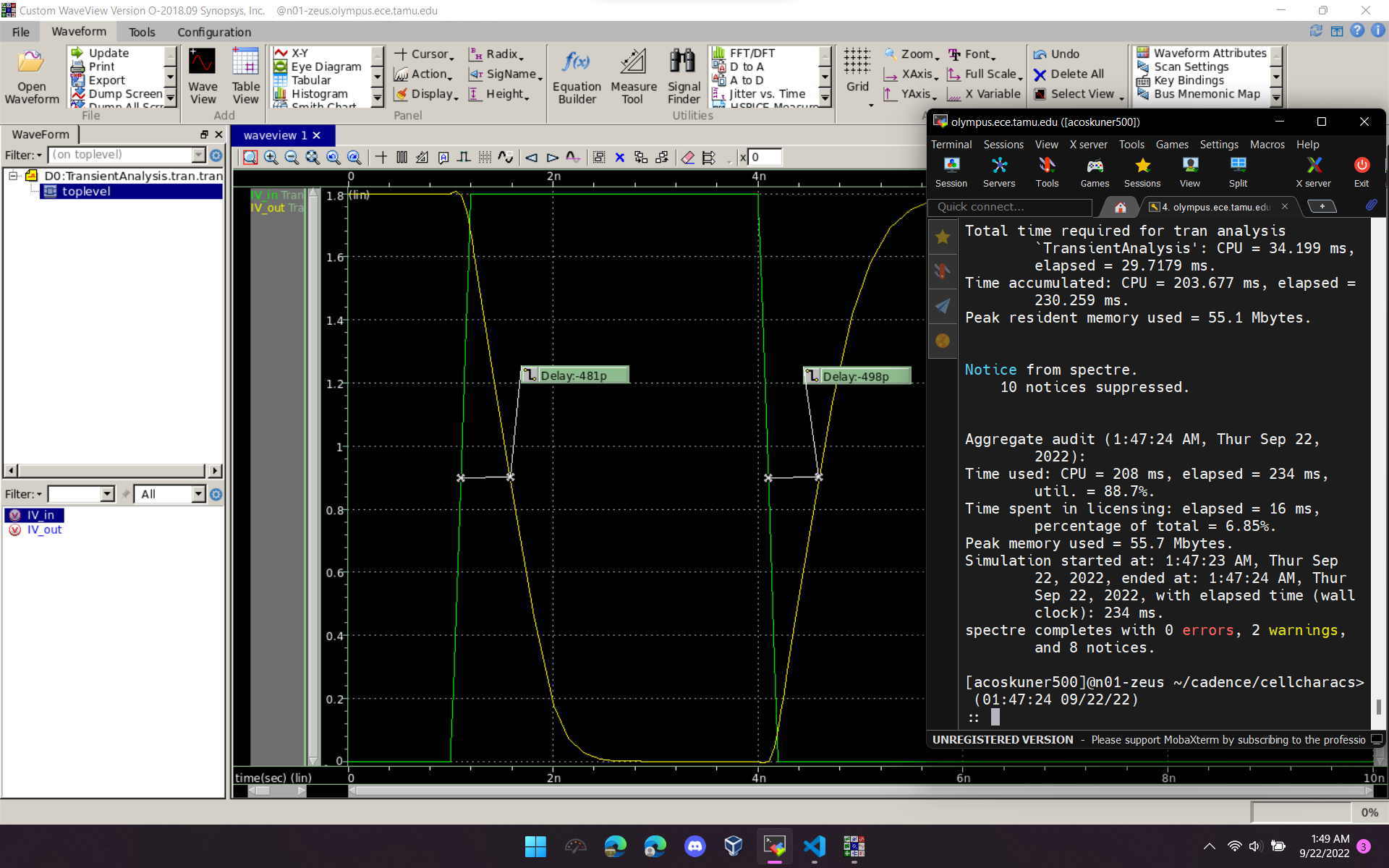
| ;Spice netlist for an inverter and a capacitorsimulator lang=spectreinclude "~/cadence/cellcharacs/model18.spi"include "~/cadence/cellcharacs/cell18.spi"vgnd (gnd 0) vsource dc=0vvdd (vdd 0) vsource dc=1.8;acinput (IV\_in 0) vsource dc=0 mag=1;acinput (NAND\_in 0) vsource dc=0 mag=1acinput (XOR\_in 0) vsource dc=0 mag=1;R1 (IV\_in IV\_in1) resistor r=0;R2 (NAND\_in NAND\_in1) resistor r=0R3 (XOR\_in XOR\_in1) resistor r=0;X1 (IV\_in1 IV\_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.4u ln=0.2u;NAND1 (NAND\_in1 vdd NAND\_out vdd gnd) NAND2 wp=0.9u lp=0.2u wn=0.4u ln=0.2uXOR1 (XOR\_in1 vdd XOR\_out vdd gnd) XOR2 wp=0.9u lp=0.2u wn=0.4u ln=0.2uFreq ac start=1e+1 stop=1e+9;save R1:currents;save R2:currentssave R3:currents |
| --- |

1. Inverter
   1. inverter.spi

| ;Spice netlist for an inverter and a capacitorsimulator lang=spectreinclude "~/cadence/cellcharacs/model18.spi"include "~/cadence/cellcharacs/cell18.spi"vgnd (gnd 0) vsource dc=0vvdd (vdd 0) vsource dc=1.8vpwl (IV\_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]X1 (IV\_in IV\_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2uR1 (IV\_out 1) resistor r=1C1 (1 0) capacitor c=100fTransientAnalysis tran start=0 stop=10ns step=1pssave IV\_in IV\_out |
| --- |

* 1. Simulation tests for <10% error

| PMOS w (μm) | NMOS w (μm) | Falling Edge Delay (ps) | Rising Edge Delay (ps) | % Error |
| --- | --- | --- | --- | --- |
| 0.6 | 0.3 | 478 | 696 | 45.6 |
| 0.9 | 0.3 | 481 | 498 | 3.53 |

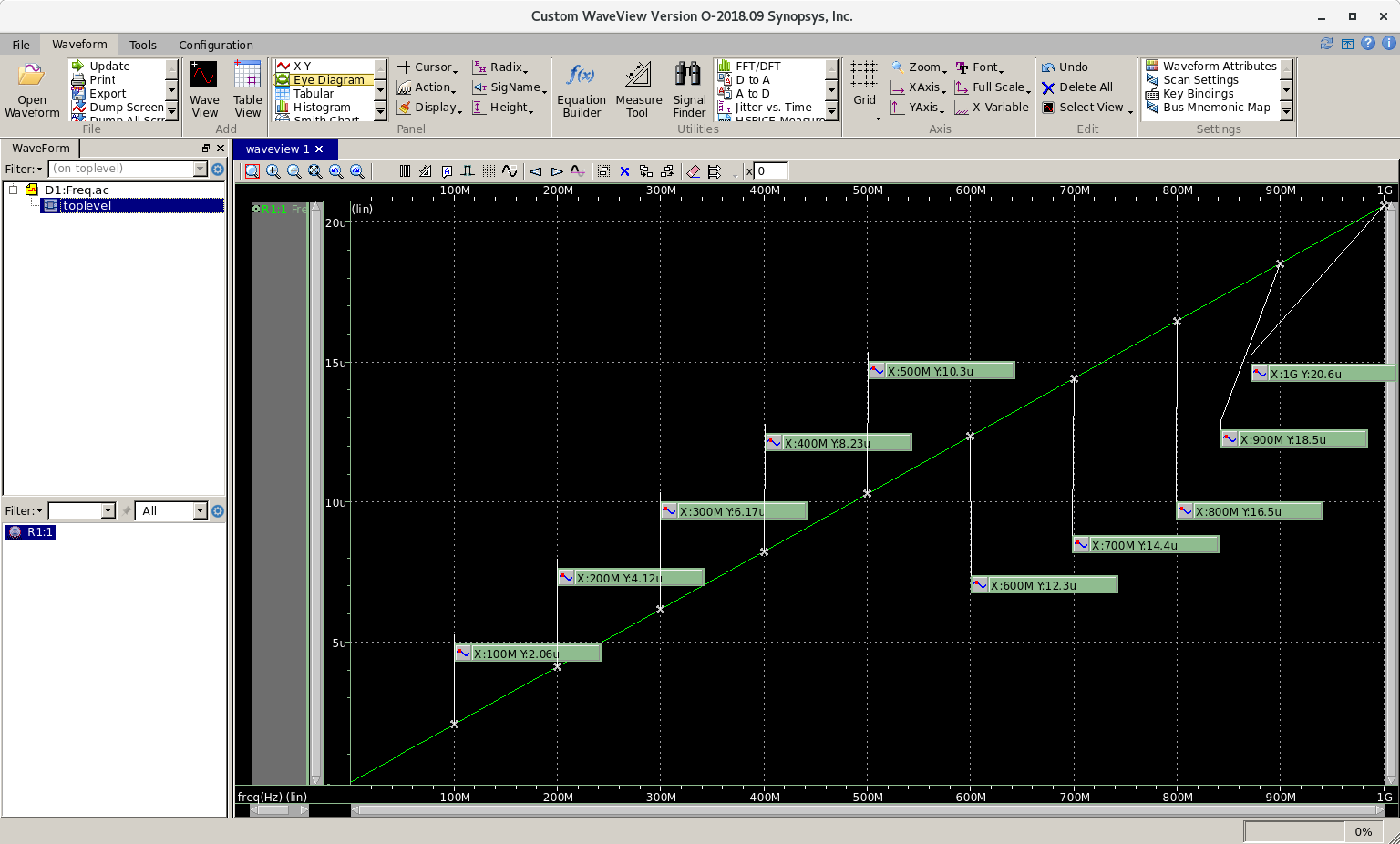


* 1. Inverter Cell Delay Table

| Output Capacitance (fF) | Falling Edge Delay (ps) | Rising Edge Delay (ps) | % Error |
| --- | --- | --- | --- |
| 100 | 481 | 498 | 3.53 |
| 90 | 439 | 451 | 2.73 |
| 80 | 393 | 410 | 4.33 |
| 70 | 351 | 368 | 4.84 |
| 60 | 306 | 321 | 4.90 |
| 50 | 262 | 277 | 5.73 |
| 40 | 219 | 232 | 5.94 |
| 35 | 197 | 210 | 6.60 |
| 30 | 175 | 188 | 7.43 |
| 25 | 153 | 166 | 8.50 |
| 20 | 131 | 144 | 9.92 |
| 15 | 109 | 122 | 11.93 |
| 10 | 85.8 | 101 | 17.72 |
| 5 | 57.7 | 74.5 | 29.12 |
| 1 | 27.1 | 45.2 | 66.79 |

* 1. Inverter Gate Capacitance (avg) = 3.275 fF

| Freq (MHz) | 100 | 200 | 300 | 400 | 500 | 600 | 700 | 800 | 900 | 1000 |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Current (μA) | 2.06 | 4.12 | 6.17 | 8.23 | 10.3 | 12.3 | 14.4 | 16.5 | 18.5 | 20.6 |
| Capacitance (fF) | 3.279 | 3.279 | 3.273 | 3.275 | 3.279 | 3.263 | 3.274 | 3.283 | 3.272 | 3.279 |

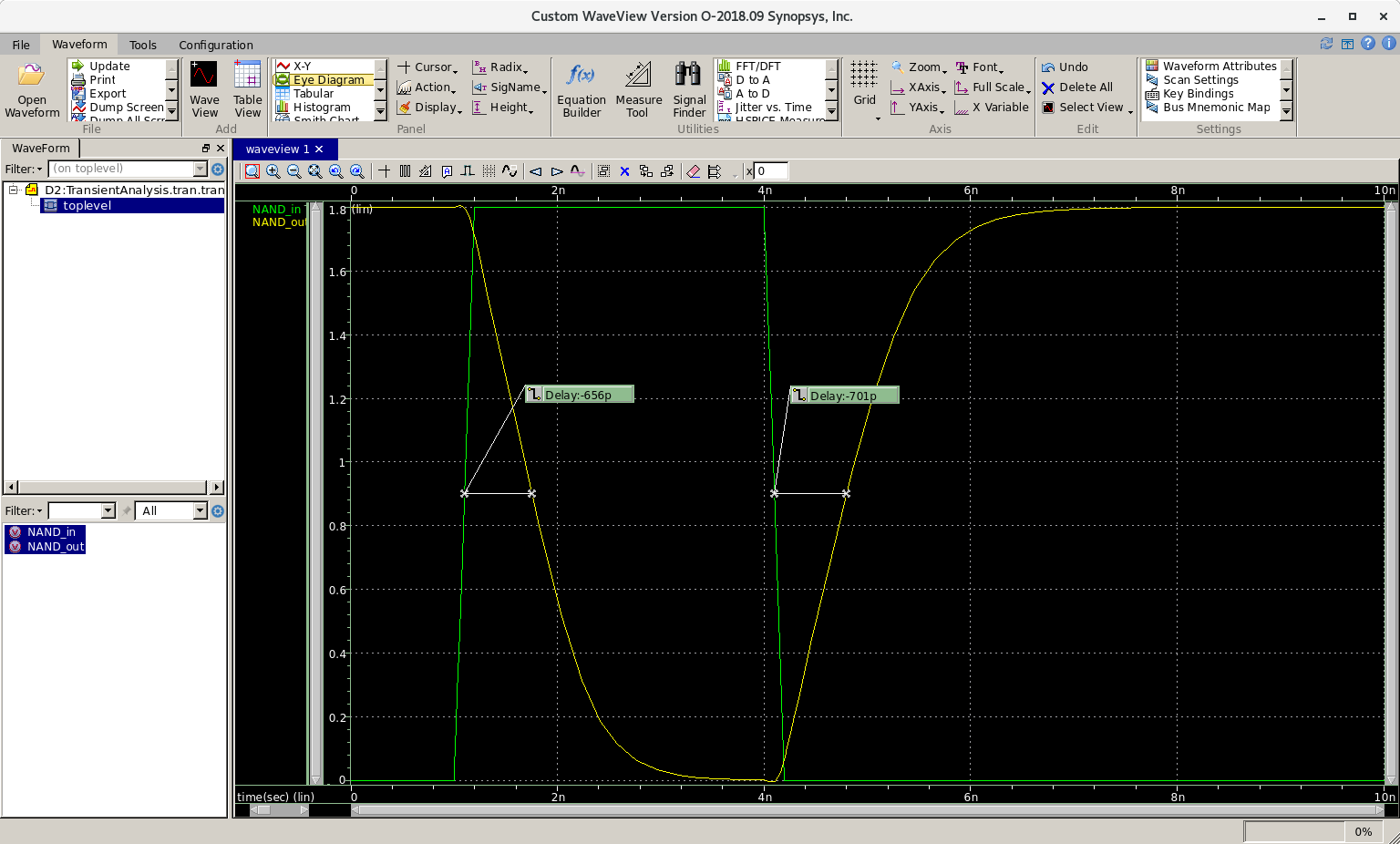


1. NAND2
   1. NAND2.spi

| ;Spice netlist for an inverter and a capacitorsimulator lang=spectreinclude "~/cadence/cellcharacs/model18.spi"include "~/cadence/cellcharacs/cell18.spi"vgnd (gnd 0) vsource dc=0vvdd (vdd 0) vsource dc=1.8vpwl (NAND\_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]NAND1 (NAND\_in vdd NAND\_out vdd gnd) NAND2 wp=0.6u lp=0.2u wn=0.3u ln=0.2uR1 (NAND\_out 1) resistor r=1C1 (1 0) capacitor c=100fTransientAnalysis tran start=0 stop=10ns step=1pssave NAND\_in NAND\_out |
| --- |

* 1. Simulation for <10% error

| PMOS w (μm) | NMOS w (μm) | Falling Edge Delay (ps) | Rising Edge Delay (ps) | % Error |
| --- | --- | --- | --- | --- |
| 0.6 | 0.3 | 656 | 701 | 6.86 |

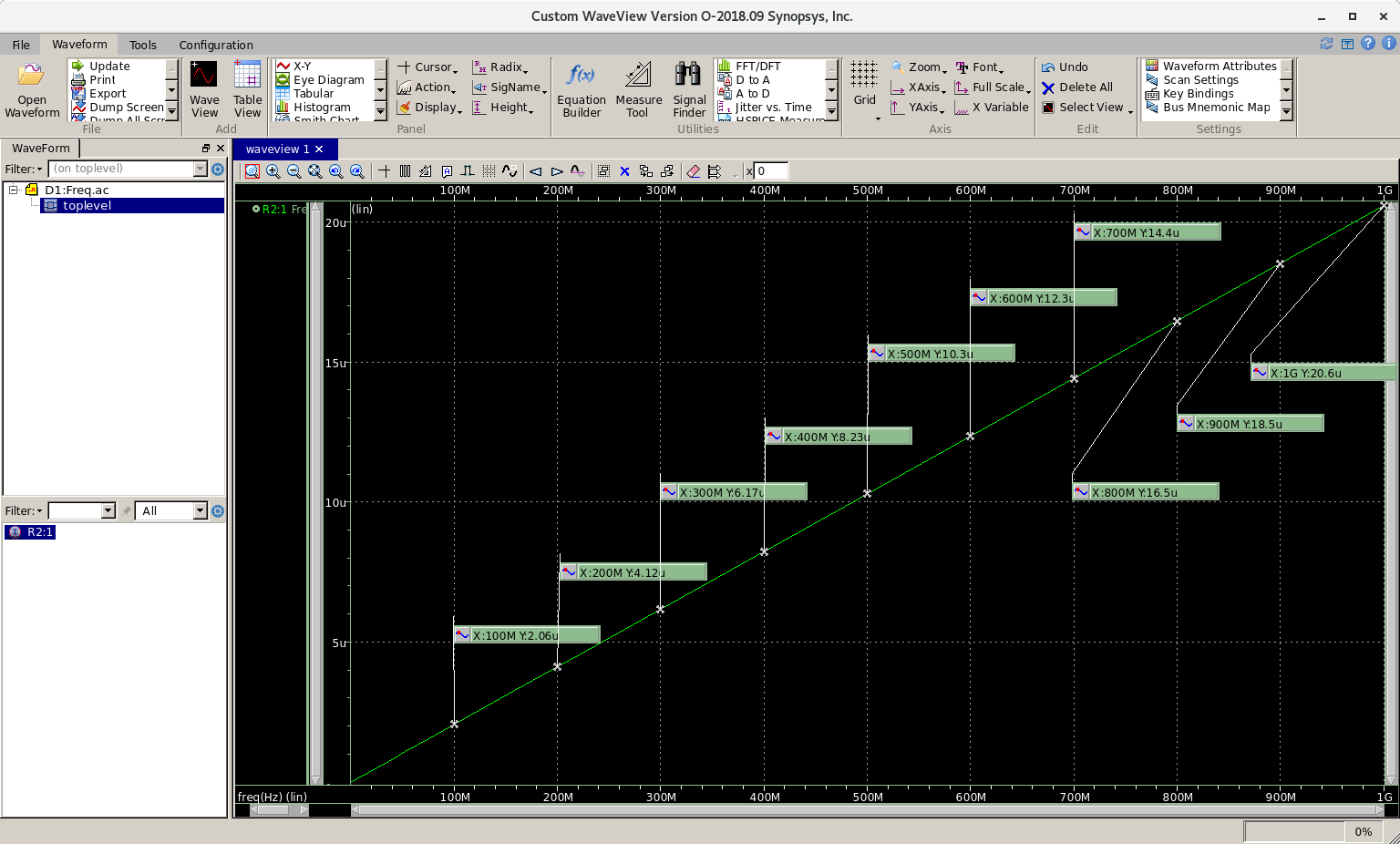


* 1. NAND2 Cell Delay Table

| Output Capacitance (fF) | Falling Edge Delay (ps) | Rising Edge Delay (ps) | % Error |
| --- | --- | --- | --- |
| 100 | 656 | 701 | 6.86 |
| 90 | 595 | 637 | 7.06 |
| 80 | 534 | 575 | 7.68 |
| 70 | 474 | 511 | 7.81 |
| 60 | 414 | 447 | 7.97 |
| 50 | 351 | 382 | 8.83 |
| 40 | 291 | 320 | 9.97 |
| 35 | 261 | 286 | 9.58 |
| 30 | 229 | 254 | 10.92 |
| 25 | 198 | 221 | 11.62 |
| 20 | 168 | 189 | 12.50 |
| 15 | 137 | 157 | 14.60 |
| 10 | 107 | 125 | 16.82 |
| 5 | 72.3 | 92.9 | 28.49 |
| 1 | 35.4 | 57.7 | 62.99 |

* 1. NAND2 Gate Capacitance (avg) = 3.275 fF

| Freq (MHz) | 100 | 200 | 300 | 400 | 500 | 600 | 700 | 800 | 900 | 1000 |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Current (μA) | 2.06 | 4.12 | 6.17 | 8.23 | 10.3 | 12.3 | 14.4 | 16.5 | 18.5 | 20.6 |
| Capacitance (fF) | 3.279 | 3.279 | 3.273 | 3.275 | 3.279 | 3.263 | 3.274 | 3.283 | 3.272 | 3.279 |

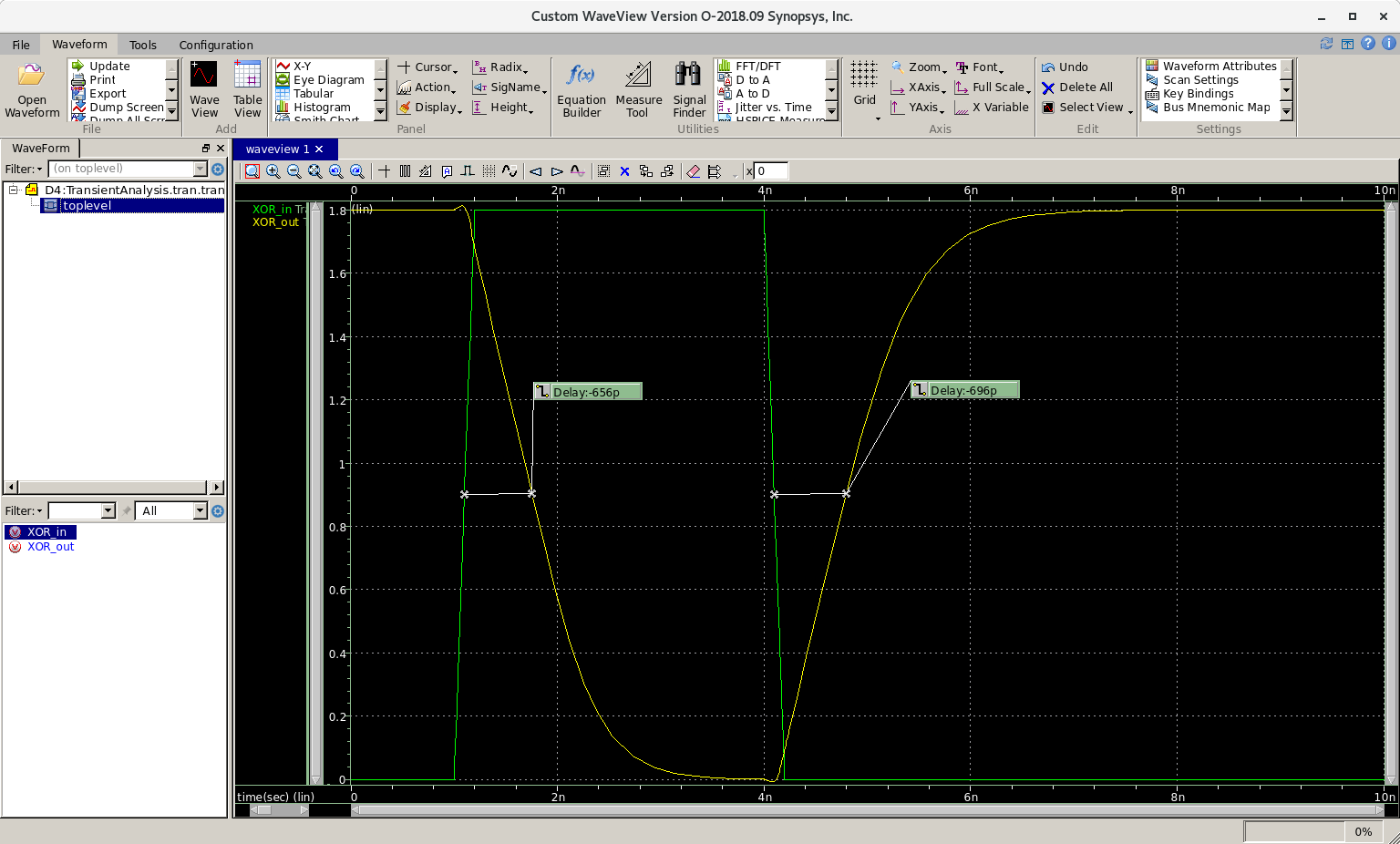


1. XOR2
   1. XOR2.spi

| ;Spice netlist for an inverter and a capacitorsimulator lang=spectreinclude "~/cadence/cellcharacs/model18.spi"include "~/cadence/cellcharacs/cell18.spi"vgnd (gnd 0) vsource dc=0vvdd (vdd 0) vsource dc=1.8vpwl (XOR\_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]XOR1 (XOR\_in vdd XOR\_out vdd gnd) XOR2 wp=1.2u lp=0.2u wn=0.3u ln=0.2uR1 (XOR\_out 1) resistor r=1C1 (1 0) capacitor c=100fTransientAnalysis tran start=0 stop=10ns step=1pssave XOR\_in XOR\_out |
| --- |

* 1. Simulation for <10% error

| PMOS w (μm) | NMOS w (μm) | Falling Edge Delay (ps) | Rising Edge Delay (ps) | % Error |
| --- | --- | --- | --- | --- |
| 0.6 | 0.3 | 649 | 1290 | 98.77 |
| 0.9 | 0.3 | 653 | 898 | 37.52 |
| 0.9 | 0.4 | 555 | 900 | 62.16 |
| 1.2 | 0.3 | 656 | 696 | 6.10 |



* 1. XOR2 Cell Delay Table

| Output Capacitance (fF) | Falling Edge Delay (ps) | Rising Edge Delay (ps) | % Error |
| --- | --- | --- | --- |
| 100 | 656 | 696 | 6.10 |
| 90 | 596 | 633 | 6.21 |
| 80 | 535 | 569 | 6.36 |
| 70 | 473 | 503 | 6.34 |
| 60 | 412 | 441 | 7.04 |
| 50 | 351 | 374 | 6.55 |
| 40 | 290 | 311 | 7.24 |
| 35 | 259 | 279 | 7.72 |
| 30 | 228 | 247 | 8.33 |
| 25 | 197 | 214 | 8.63 |
| 20 | 166 | 182 | 9.64 |
| 15 | 134 | 149 | 11.19 |
| 10 | 103 | 117 | 13.59 |
| 5 | 70.4 | 81.7 | 16.05 |
| 1 | 41.3 | 51.3 | 24.21 |

* 1. XOR2 Gate Capacitance (avg) = 6.548 fF

| Freq (MHz) | 100 | 200 | 300 | 400 | 500 | 600 | 700 | 800 | 900 | 1000 |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Current (μA) | 4.12 | 8.23 | 12.3 | 16.5 | 20.6 | 24.7 | 28.8 | 32.9 | 37 | 41.1 |
| Capacitance (fF) | 6.557 | 6.549 | 6.525 | 6.565 | 6.557 | 6.552 | 6.548 | 6.545 | 6.543 | 6.541 |

